Remarks

Reconsideration of the application is requested. Applicants appreciate the allowance of claims 1-21, 26, and 27 and the objection to claim 25. However, for at least the following reasons, applicants respectfully traverse the rejections of claims 22-24 as unpatentably obvious over Anderson in view of Aung and claims 28-32 as anticipated by Anderson.

Claim 22

Claim 22 recites a digital phase locked loop (DPLL) that includes, among other things, a digital filter:

> wherein the digital filter includes at least one reloadable register operable to store a programmable value for comparison with a value derived from the up and down signals and a controller responsive to the comparison and operable to generate the FWD and BWD signals.

The Examiner mistakenly cites portions of Aung as disclosing this feature of the claim, pointing to shift register 200 (paragraphs [0060-0061] and FIG. 5) and PLL 100 (paragraph [0044] and FIG. 2). These structures, though, are not related to a digital phase locked loop (DPLL). As paragraphs [0060-0061] and FIG. 5 make clear, shift register 200 is part of deserializer 60 (FIG. 5), which is separate and distinct from Aung's CDR 50 (FIG. 1) and its DPLL 150 (FIG. 4). PLL 100 (FIG. 2), although part of CDR 50, is also separate and distinct from DPLL 150.

Aung's DPLL is shown in FIG. 4 and described in paragraphs [0051-0054]. Of particular relevance is the following passage in paragraph [0053]:

> However, state machine 162 does not produce output signal pulses in response to every UP and DOWN signal pulse it receives. Instead, state machine 162 outputs further UP and DOWN signal pulses only after a trend has emerged in the signals it receives. In other words, state machine 162 acts somewhat like a digital low-pass filter to prevent the rest of the FIG. 4 circuitry from responding too quickly to what may turn out to be only a short term indication of phase mismatch produced by phase detector 160. State machine 162 therefore builds some desirable latency into the circuitry shown in FIG. 4.

Nowhere in this passage (or elsewhere in Aung) is there any suggestion that state machine 162 is programmable. Lacking such suggestion, Aung cannot be said to teach or suggest the programmable limitation of claim 22.

Claims 28 and 32

In rejecting these claims, applicants believe that the Examiner incorrectly equates a predefined value with a programmable value. A predefined value is a fixed value that cannot be changed; a programmable value by its nature can be changed. Anderson is an example of a prior art digital filter described in the present application at page 8, line 16 to page 9, line 6. Such a digital filter cannot accommodate multiple communication protocols because it compares a predefined count value (not programmable) with a value derived from the actual count of up and down signals. (Anderson, col. 3, lines 22-28). In contrast, the claimed methods include "comparing a programmable value with the derived value" (claim 28) or "comparing the difference value to a first programmable value" and "comparing the sum value to a second programmable value" (claim 32). By using a programmable value, the claimed methods can do what Anderson cannot – receive and process high-speed serial data of various protocols using a single digital filter if desired.

New Claim 33

Claim 33 is similar to claim 22 but emphasizes more the programmable nature of the digital filter's characteristics, specifically the use of a programmable bandwidth parameter with the up and down signals to generate the FWD and BWD signals.

For the reasons stated above, applicants submit therefore that the present claims are patentable over the art of record and that the application is now in condition for allowance.

Please call the undersigned if he can be of any further assistance in this case.

Respectfully submitted,

Date: 5/26/05

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